

I CLAIM:

1. Apparatus for use in a reduced clock finite impulse response (FIR) filter comprising:
 - i) a multiplexer/multiplier (mux/mul) means having Q inputs and one output;
 - ii) selection means for controlling said mux/mul means operative to produce said
5 one output from one of said Q inputs; and
 - iii) output conditioning means coupled to the output of said mux/mul means to produce a conditioned output signal corresponding to a coefficient used in an FIR filter.
2. The apparatus of claim 1 wherein said signal conditioning means modifies the gain
10 and the sign of the output of the corresponding mux/mul.
3. The apparatus of claim 2 further including means to produce a clock signal at the data rate of a data signal coupled to said selection means wherein said clock signal controls the selected output of said selection means from one of said Q inputs.
4. Apparatus for use in a reduced clock rate finite impulse response filter comprising:
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 - i) Q latch means all coupled to an input data signal having a unit interval rate and each latch means providing a latched output signal in response to a latch control signal;
 - ii) Q multiplexer/multiplier (mux/mul) means, each mux/mul means providing one output and Q inputs to receive the latched output signal of a respective latch means; and
 - iii) selection means for controlling said mux/mul means operative to produce an
20 output signal selected from one of said Q inputs.
5. The apparatus of claim 4 further including:
 - i) signal conditioning means for each mux/mul means to condition the output signal of the mux/mul means; and
 - ii) summing means to sum the conditioned signals of all such signal conditioning
25 means.
6. The apparatus of claim 5 wherein said signal conditioning means modifies the gain and the sign of the output signal of the corresponding mux/mul means.
7. The apparatus of claim 4 further including:

i) means to produce a clock signal;

ii) Q phase delay means coupled to said clock signal providing an output latch control signal to a corresponding latch means.

8. The apparatus of claim 7 wherein each phase delay means produces a unique output
5 latch control signal that is phase delayed from the clock signal by a phase delay of $N \times 360/Q$, where unique values of N correspond to each individual phase delay means and range from 0 to Q-1;

9. The apparatus of claim 7 wherein the means to produce a clock signal operates to
10 produce a clock signal that is a sub-multiple Q of the unit interval rate of said input data signal.

10. The apparatus of claim 4 wherein the selection means operates to select an output
signal from one of said Q inputs at a rate corresponding to the unit interval rate of said input
data signal.

11. In a transversal finite impulse response (FIR) filter for processing data bits that are
15 shifted through delay elements at reference clock rate and each delay element is coupled to a
corresponding multiplier and all of the multiplied outputs are summed, the improvement
comprising:

i) a column of delay elements arranged to form Q rows for processing data bits
20 that are shifted through delay elements of each row at a shift rate that is a sub-multiple Q of
the reference clock rate;

ii) Q multiplexer/multiplier (mux/mul) means having Q inputs each
correspondingly coupled to a delay element in said column of delay elements and each said
mux/mul produces one output from one of said Q inputs; and

25 iii) selection means for controlling said mux/mul means operative to select said
one output of said Q inputs at said reference clock rate,
wherein said selected output of a mux/mul is provided to the corresponding multiplier and
summed in the transversal FIR filter.

12. A method for providing a feed forward equalizer (FFE) in a transversal finite impulse response (FIR) filter for transmitting data bits that are shifted through delay elements at a reference clock rate defining a unit interval period and each delay element is coupled to a corresponding multiplier and all of the multiplied outputs are summed, comprising the steps of:

i) supplying the data bits to be processed to Q shift registers operating at a shift rate that is the quotient of the reference clock rate divided by Q; and

ii) multiplexing said Q shift registers to a FIR FFE multiplier summing network for a unit interval period defined by said reference clock rate such that each shift register of said Q shift registers is successively multiplexed to the FIR FFE multiplier summing network in successive unit interval periods.

13. A method for providing a decision feedback equalizer (DFE) in a transversal finite impulse response (FIR) filter for recovering data bits in a received data signal having a data rate defining a unit interval period comprising the steps of:

i) conditioning the received data signal;

ii) supplying the conditioned data signal to Q shift registers of a DFE network, all said shift registers operating at a shift rate that is the quotient of the clock rate of the received data signal divided by Q; and

iii) multiplexing said Q shift registers to a FIR DFE multiplier summing network for a unit interval period defined by said clock rate of the received data signal such that each shift register of said Q shift registers is successively multiplexed to the FIR DFE multiplier summing network in successive unit interval periods.